Remarks/Arguments

This Amendment is in response to the Office Action mailed July 18, 2006. In this Office Action, the Examiner rejected claims 17, 21 and 24-27 under 35 USC 112, 2nd paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Further, the Examiner rejected claims 16-27 under 35 USC 102(e) as being anticipated by Elabd (US Pat. No. 6,526,462).

For the Examiner's convenience, a clean list of the claims is attached in Appendix A.

1. Claim Rejections under 35 USC 112, 2nd Paragraph

The Examiner rejected claims 17, 21 and 24-27 under 35 USC 112, 2nd Paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. The Applicant is amending those claims in this amendment. Therefore, the Applicant respectfully requests that the Examiner withdraw the rejections to claims 17, 21 and 24-27 under 35 USC 112, 2nd Paragraph.

2. Claim Rejections under 35 USC 102(e)

The Examiner rejected claims 16-27 under 35 USC 102(e) as being anticipated by Elabd (US Pat. No. 6,526,462). After reviewing the Office Action and the Examiner's comments, the Applicant is amending the claims to better clarify the claimed invention.

The Examiner found that Elabd shows and teaches all of the elements of the claimed invention. Applicant disagrees with the Examiner and finds that Elabd is not a proper 102(e) reference because it does contain all of the elements of Applicant's claimed invention.

Elabd describes a highly intelligent programmable multi-tasking memory management system manages memory requests associated with a system on chip (SOC) device. The memory management system includes a routing controller or central processing unit (RCPU) that is used for routing/switching stream data between communication cores and digital signal processors with minimum reliance and demand on a main or virtual central processing unit (VCPU) residing on a system bus. Tasks are partitioned between the VCPU and the RCPU within the SOC architecture for communication applications. The VCPU performs system/application tasks while the RCPU simultaneously performs multiple memory routing/switching tasks and multiple concurrent memory access connections.

From an implementation standpoint, Elabd teaches that all incoming requests are stored in a large request buffer (referred to in claim 5, where the memory management processing includes as quoted in the patent, "inputting memory requests from the plurality of communication cores to a request buffer", then "outputting the memory

requests from the request buffer to a foreground request schedule and a background request schedule followed by queuing the memory requests in the background request schedule, and processing simultaneously as predetermined number of requests." Essentially, all of the incoming requests are internally buffered in the Elabd memory management system, then distributed in parallel to the different memory banks or are buffered internally to be sent later.

Elabd's approach has advantages such as buffering the requests allows for the additional claims of being able to process, analyze, and distribute requests (using the "routing CPU" as detailed in Elabd) and also check for coherency. This approach however requires both a large memory buffer (Elabd uses a SRAM buffer) and a separate routing CPU to both process and analyze the requests, and for many applications this may be overkill, requiring too much hardware and greatly increasing the cost of the system. The Application describes the type of system in paragraphs 19 through 21.

Since Elabd buffers, processes and schedules the different memory requests, there is inherent latency for each request getting serviced by the memory target, which may be on the order of many cycles, which may not be acceptable for certain designs and applications. With the "Flexible Matrix Fabric", the request is routed straight through to the memory target, with only delays being any register pipelining stages added for timing issues. In some implementations the matrix can actually just pass requests straight to the memory target if pipelining is not required, resulting in no latency lost across the fabric.

Elabd's approach also describes a tightly integrated system of the buffer, arbitration and memory targets rather than an open flexible system of the Matrix Fabric. Arbitration in Elabd's architecture is tightly coupled in the Memory Management System. Claim 7 of Elabd teaches that "foreground requests correspond go requests residing in an SRAM buffer." Claim 8 specifies both a multiplexer for selecting a predetermined number of peripheral memory requests from the plurality of peripheral masters, and also a multi tasking arbiter and load balancing system coupled to the multiplexer and adapted to provide an arbitration, load balancing and scheduling scheme to the multiplexer.

The claimed invention, on the other hand, describes a System-on-Chip (SOC) interconnection method and apparatus that discloses an internal switching fabric that interconnects, via standard connection ports, one or more requestors and one or more addressable targets on a single semiconductor integrated circuit. The claimed invention is designed to overcome the problems associated with the Elabd system. The Application describes the differences between the claimed invention and the Elabd system in paragraph 22 of the application. Paragraph 23 of the application illustrates that the Elabd system does not have the flexibility of the claimed invention. And, paragraphs 24 through 29 describes the advantages that the claimed invention has over the Elabd system.

Referring now to specific differences between the claimed invention and Elabd, Elabd requires a large request buffer structure to handle/buffer incoming requests so as to function. The claimed invention does not have this element.

Elabd contains a single, centralized RCPU for routing and switching data. The Examiner incorrectly asserts that Elabd's RCPU was the same as the claimed invention's decoder/router element. This is incorrect because there could be multiple router/decoder elements depending on the SOC'S design. For each requester in the design, there will be a corresponding decoder/router element. In an Elabd system, there is only one RCPU. In addition, the router/decoder element of the claimed invention is able to translate between a requester bus protocol and a possibly different target bus protocol. This feature is not described in Elabd.

Elabd requires a VCPU to co-ordinate tasks with the RCPU to enable its operation. The claimed invention does have this element.

Elabd requires a multitasking arbiter to perform a required arbitration for this device to operate. An arbiter and arbitration is optional in the claimed invention for it to operate.

Elabd requires a load balancing system for enabling the selection of a predetermined number of peripheral memory requests. The claimed invention does not have this element.

And, the Examiner incorrectly asserts that the unique predefined address space element and the internal system memory map element of the claimed invention are a single equivalent structure to Elabd's memory mapping element. The internal system memory map element and the unique predefined address space element are separate components with separate functions. In addition, each individual decoder/router element contains its own internal system memory map. If there are multiple requesters, which

means that there are multiple decoder/router elements, then the claimed invention will comprise multiple internal system memory maps (one for each decoder/router element). Thus, the Examiner incorrectly construes this internal system memory map to be equivalent to the single centralized memory mapping element in Elabd.

Since the amended claims include elements and limitations that are not shown, taught, or implied by the Elabd, and in addition, the claimed invention does not contain elements or limitations as required by Elabd, Applicant therefore respectfully requests that the Examiner withdraw the claim rejections to claims 16-27 under 35 USC 102(e) as being anticipated by Elabd (US Pat. No. 6,526,462)

3. Summary

In view of the above, Applicant believes that each of the presently pending claims is in immediate condition for allowance or appeal. Accordingly, Applicant respectfully requests that the Examiner withdraw the outstanding objections and rejections of the claims and issue a timely Notice of Allowance in this case.

Respectfully submitted,
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